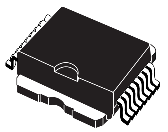
VNQ05XSP16

QUAD CHANNEL HIGH SIDE SOLID STATE RELAY

TYPE	R_{ON}(*)	I_{OUT}	V_{CC}
VNQ05XSP16	110mΩ	5A (*)	36 V

(*) Per each channel

- OUTPUT CURRENT (CONTINUOUS): 5A
- CMOS COMPATIBLE INPUTS
- MULTIPLEXED PROPORTIONAL LOAD CURRENT SENSE
- UNDERVOLTAGE & OVERVOLTAGE SHUT- DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT DOWN
- CURRENT LIMITATION
- VERY LOW STAND-BY POWER DISSIPATION
- PROTECTION AGAINST: LOSS OF GROUND & LOSS OF V_{CC}
- REVERSE BATTERY PROTECTION (**)



PowerSO-16™

ORDER CODES		
PACKAGE	TUBE	T&R
PowerSO-16™	VNQ05XSP16	VNQ05XSP1613TR

DESCRIPTION

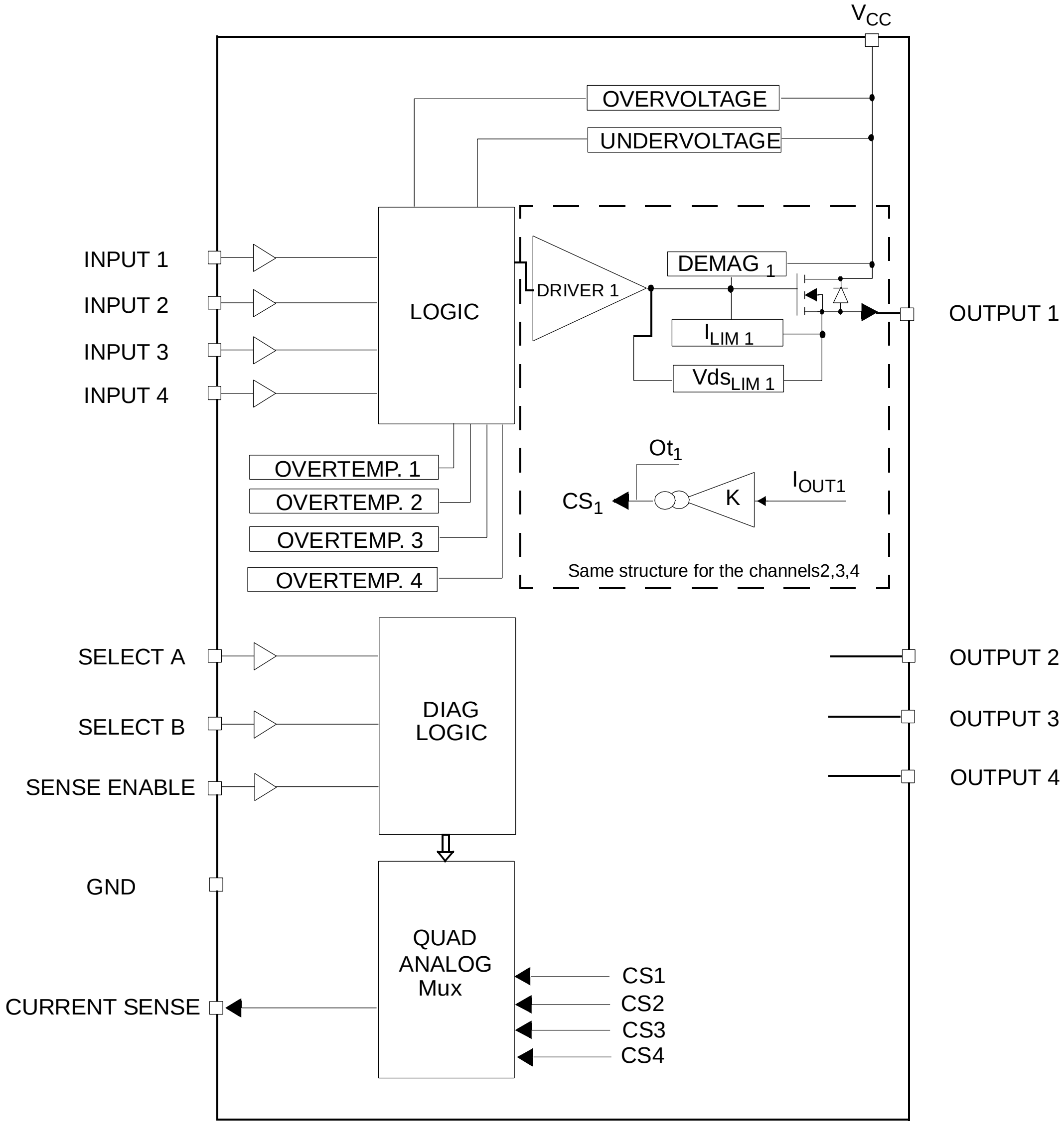
The VNQ05XSP16 is a monolithic device designed in STMicroelectronics VIPower M0-3 Technology. It is intended for driving any type of multiple loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). This device has four independent channels and one multiplexed analog sense output which deliver a current proportional to the selected output current. SenseEnable pin allows to connect any number of VNQ05XSP16 on the same Current Sense line. Active current limitation combined with thermal shut-down and automatic restart protect the device against overload. Device automatically turns off in case of ground pin disconnection.

ABSOLUTE MAXIMUM RATING

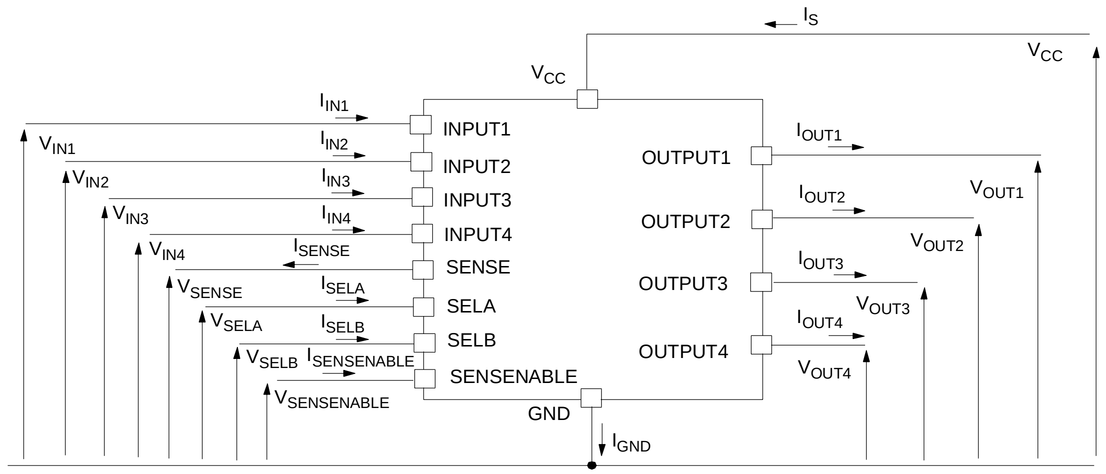
Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (continuous)	41	V
$-V_{CC}$	Reverse supply voltage (continuous)	-0.3	V
I_{OUT}	Output current (continuous), for each channel	Internally limited	A
I_R	Reverse output current (continuous), for each channel	-5	A
I_{IN}	Input current (IN1,IN2,IN3,IN4,SELA,SELB,SENSENABLE)	+/- 10	mA
V_{CSENSE}	Current sense maximum voltage	-3	V
		+15	V
I_{GND}	Ground current at $T_{case} \leq 25°C$ (continuous)	-200	mA
V_{ESD}	Electrostatic Discharge (Human Body Model: R=1.5Ω; C=100pF)		
	- INPUT	4000	V
	- CURRENT SENSE	2000	V
	- OUTPUT	5000	V
	- V_{CC}	5000	V
P_{tot}	Power dissipation at T_{case}=25°C	78	W
E_{MAX}	Maximum Switching Energy (L=1.72mH; R_L=0Ω; V_{bat}=13.5V; T_{jstart}=150ºC; I_L=7.5A)	76	mJ
T_j	Junction operating temperature	Internally limited	°C
T_c	Case Operating Temperature	- 40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

(**) See application schematic at page 9

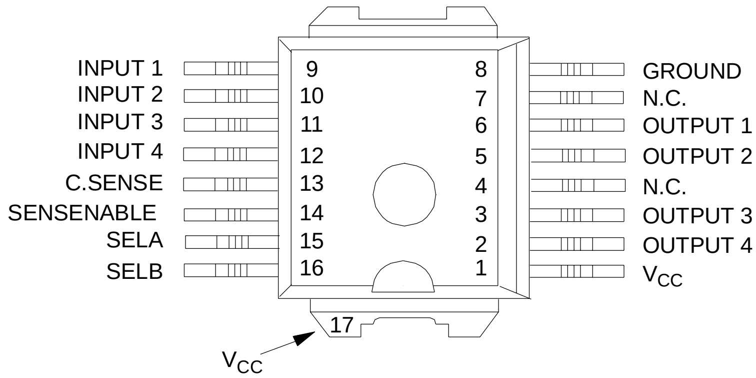
BLOCK DIAGRAM



CURRENT AND VOLTAGE CONVENTIONS



CONNECTION DIAGRAM (TOP VIEW)



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	(MAX)	1.6	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	(MAX)	51.6 (*)	°C/W

(*) When mounted on FR4 printed circuit board with 0.5 cm² of copper area (at least 35 µm thick) connected to all V_{CC} pins

ELECTRICAL CHARACTERISTICS (8V<V_{CC}<36V; -40°C<T_j<150°C; unless otherwise specified) (Per each channel)
POWER

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Under voltage shut down		3	4	5.5	V
V_{OV}	Overvoltage shut down		36			V
R_{ON}	On state resistance	I_{OUT}1,2,3,4=1A; T_j=25°C I_{OUT}1,2,3,4=1A; T_j=150°C I_{OUT}1,2,3,4=0.5A; V_{CC}=6V			110 220 330	mΩ mΩ mΩ
V_{clamp}	Clamp Voltage	I_{CC}=20mA (See note 1)	41	48	55	V
I_S	Supply current	Off state; Inputs=n.c.; V_{CC}=13V On state; V_{IN}=5V; V_{CC}=13V; I_{OUT}=0A; R_{SENSE}=3.9kΩ			80 10	µA mA
$I_{L(off1)}$	Off State Output Current	V_{IN}=V_{OUT}=0V	0		50	µA
$I_{L(off2)}$	Off State Output Current	V_{IN}=0V; V_{OUT}=3.5V	-75		0	µA
$I_{L(off3)}$	Off State Output Current	V_{IN}=V_{OUT}=0V; Vcc=13V; T_j=125°C			5	µA
$I_{L(off4)}$	Off State Output Current	V_{IN}=V_{OUT}=0V; Vcc=13V; T_j=25°C			3	µA

SWITCHING (V_{CC}=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	R_L=2.6Ω channels 1,2,3,4 (see figure 2)		40		µs
$t_{d(off)}$	Turn-off delay time	R_L=2.6Ω channels 1,2,3,4 (see figure 2)		40		µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L=2.6Ω channels 1,2,3,4 (see figure 2)		See relative diagram		V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L=2.6Ω channels 1,2,3,4 (see figure 2)		See relative diagram		V/µs

PROTECTIONS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{lim}	DC short circuit current	V_{CC}=13V 5.5V<V_{CC}<36V	5	7.5	10 10	A A
T_{TSD}	Thermal shut down temperature		150	175	200	°C
T_R	Thermal reset temperature		135			°C
T_{HYST}	Thermal hysteresis		7	15		°C
V_{demag}	Turn-off output voltage clamp	I_{OUT}=2A; L=6mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V
V_{ON}	Output voltage drop limitation	I_{OUT}=0.1A T_j=-40°C...+150°C		50		mV

Note 1: V_{clamp} and V_{OV} are correlated. Typical difference is 5V.

CURRENT SENSE (9V< V_{CC} <16V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT}=0.1A; V_{SENSE}=0.5V T_j=-40...+150°C	650	950	1200	
dK_1/K_1	Current Sense Ratio Drift	I_{OUT}=0.1A; V_{SENSE}=0.5V; T_j= -40°C...+150°C	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT}=1.0A, V_{SENSE}=4V T_j=-40...+150°C	800	1000	1200	
dK_2/K_2	Current Sense Ratio Drift	I_{OUT}=1.0A; V_{SENSE}=4V; T_j=-40°C...+150°C	-8		+8	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT}=2.0A, V_{SENSE}=4V T_j=-40...+150°C	850	1000	1150	
dK_3/K_3	Current Sense Ratio Drift	I_{OUT}=2.0A; V_{SENSE}=4V; T_j=-40°C...+150°C	-6		+6	%
I_{SENSEO}	Analog Sense Leakage Current	V_{CC}=6...16V; I_{OUT}=0A;V_{SENSE}=0V; T_j=-40°C...+150°C	0		10	µA
$V_{SENSE1,2,3,4}$	Max analog sense output voltage	V_{CC}=5.5V, $I_{OUT1,2,3,4}$=1.0A R_{SENSE}=10kΩ V_{CC}>8V, $I_{OUT1,2,3,4}$=2.0A R_{SENSE}=10kΩ	2 4			V V
V_{SENSEH}	Analog sense output voltage in overtemperature condition	V_{CC}=13V; R_{SENSE}= 3.9kΩ		5.5		V
$R_{VSENSEH}$	Analog sense output impedance in overtemperature condition	V_{CC}=13V; Tj>T_{TSD}; All Channels Open		400		Ω
t_{DSENSE}	Current sense delay	V_{CC}=13V; R_{SENSE}=3.9kΩ (see note 2)		300	500	µs

LOGIC CHARACTERISTICS (Inputs, Sela&b, Sensenable)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage				1.25	V
V_{IH}	Input high level voltage		3.25			V
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
I_{IL}	Low level input current	V_{IN}=1.25V	1			µA
I_{IN}	High level input current	V_{IN}=3.25V			10	µA
V_{ICL}	Input clamp voltage	I_{IN}=1mA I_{IN}=-1mA	6	6.8 -0.7	8	V V

Note 2: current sense signal delay after positive input slope.

Note: Sense pin doesn't have to be left floating.

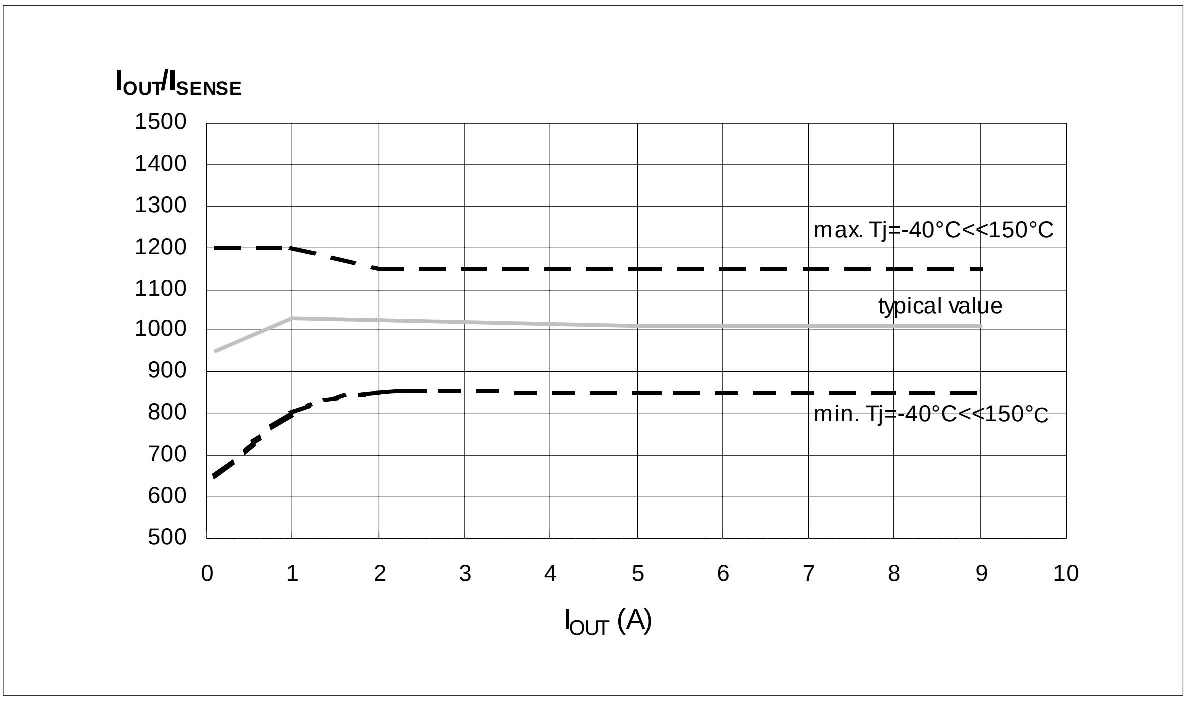
TRUTH TABLE

CONDITIONS	INPUT	OUTPUT	SENSE
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overvoltage	L H	L L	0 0
Short circuit to GND	L H H	L L L	0 $(T_j<T_{TSD})$ 0 $(T_j>T_{TSD})$ V_{SENSEH}
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

TRUTH TABLE

SENSENABLE	SELB	SELA	SENSE
L	X	X	High Impedance
H	L	L	$I_{SENSE}=I_{OUT1}/K$
H	L	H	$I_{SENSE}=I_{OUT2}/K$
H	H	L	$I_{SENSE}=I_{OUT3}/K$
H	H	H	$I_{SENSE}=I_{OUT4}/K$

Figure 1: I_{OUT}/I_{SENSE} versus I_{OUT}



ELECTRICAL TRANSIENT REQUIREMENTS

ISO T/R 7637/1 Test Pulse	Test Levels I	Test Levels II	Test Levels III	Test Levels IV	Test Levels Delays and Impedance
1	-25V	-50V	-75V	-100V	2ms, 10Ω
2	+25V	+50V	+75V	+100V	0.2ms, 10Ω
3a	-25V	-50V	-100V	-150V	0.1µs, 50Ω
3b	+25V	+50V	+75V	+100V	0.1µs, 50Ω
4	-4V	-5V	-6V	-7V	10ms, 0.01Ω
5	+26.5V	+46.5V	+66.5V	+86.5V	400ms, 2Ω

ISO T/R 7637/1 Test Pulse	Test Levels Result I	Test Levels Result II	Test Levels Result III	Test Levels Result IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 2: Switching Characteristics (Resistive load R_L=1.3Ω)

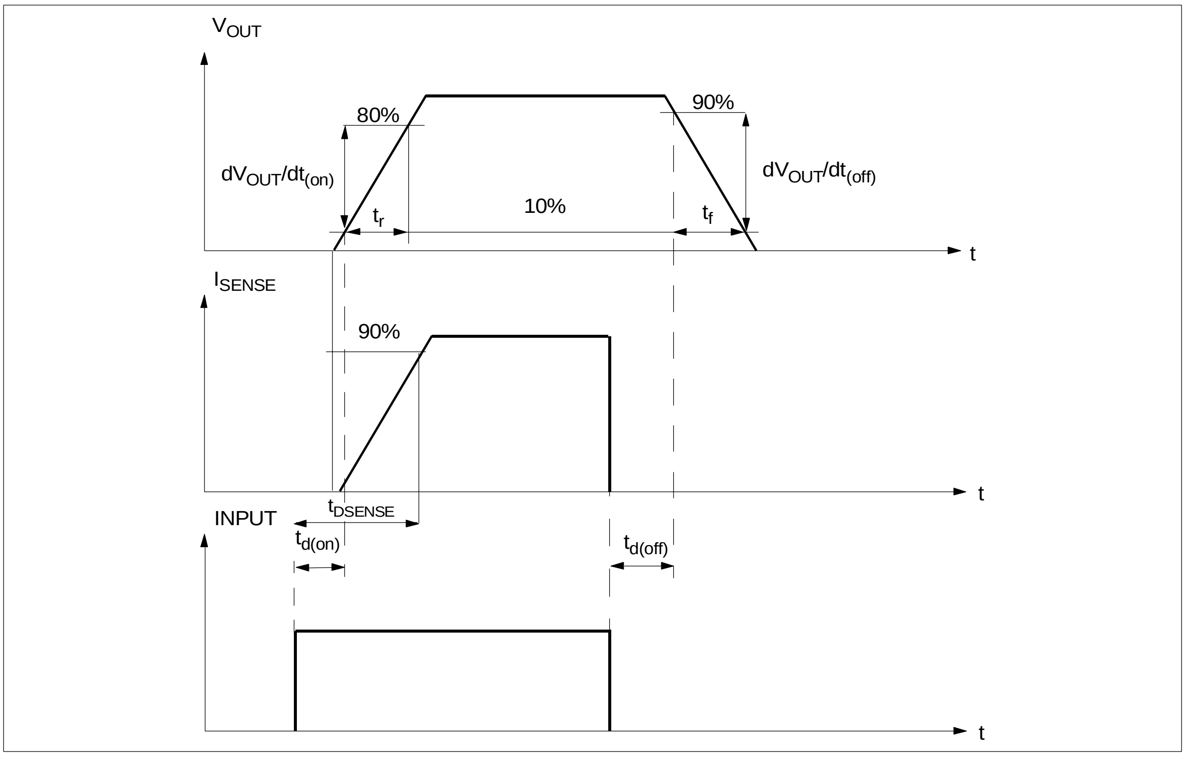
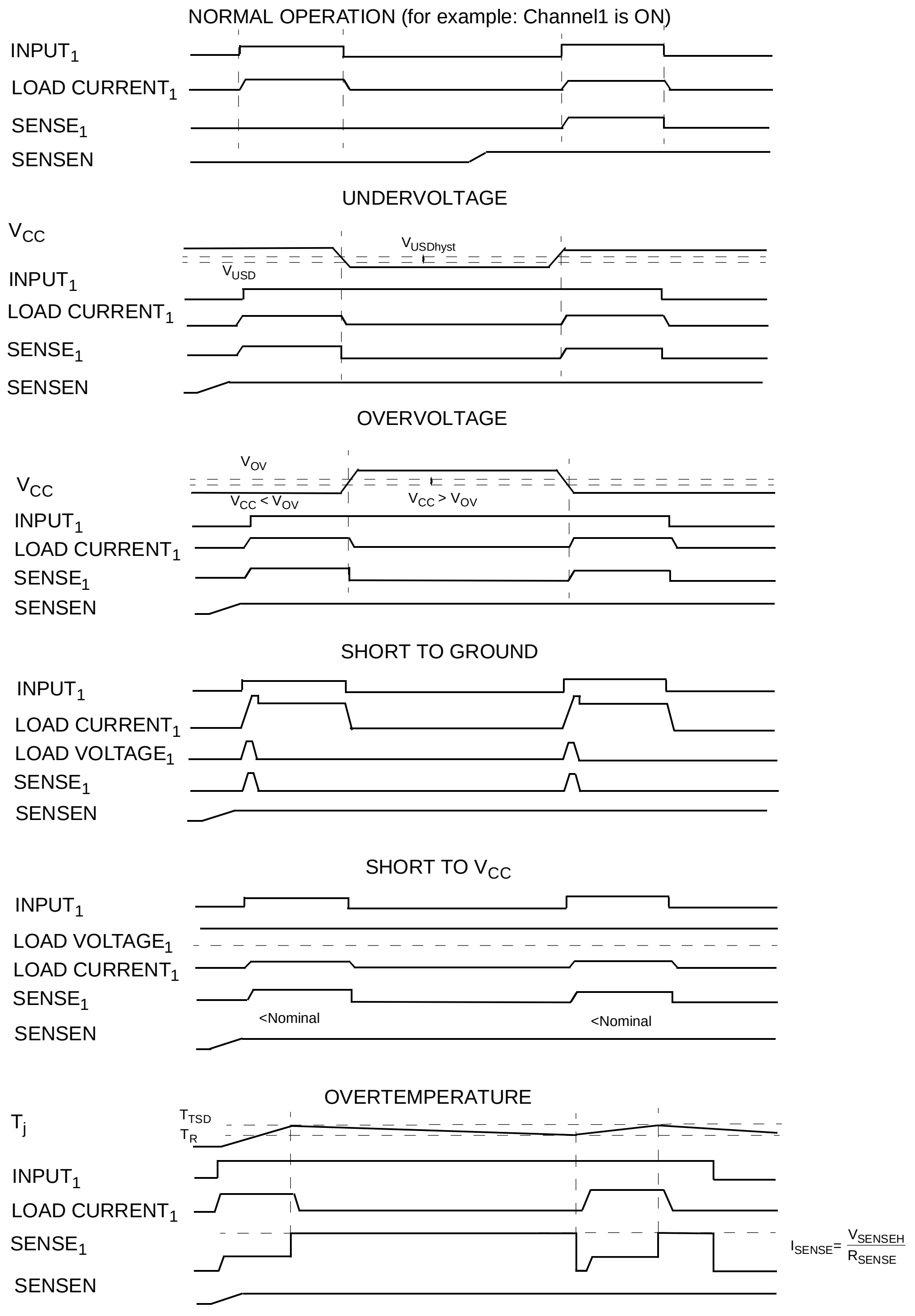
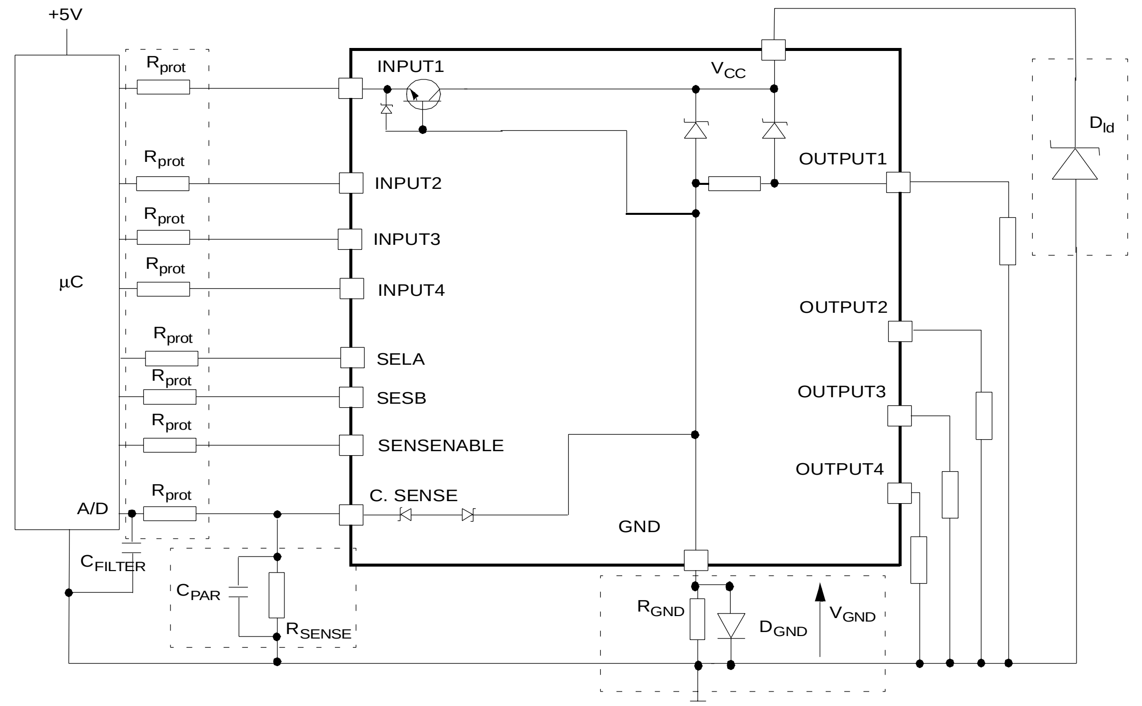


Figure 3: Waveforms



APPLICATION SCHEMATIC



Notes: Input1,2,3,4, SELA, SELB, SENSENABLE have the same structure.
$R_{SENSE} \times C_{PAR} < 10\mu s$

GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1) $R_{GND} \leq 600mV / (I_{S(on)max})$.

2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$P_D = (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (≅600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

LOAD DUMP PROTECTION

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

μC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

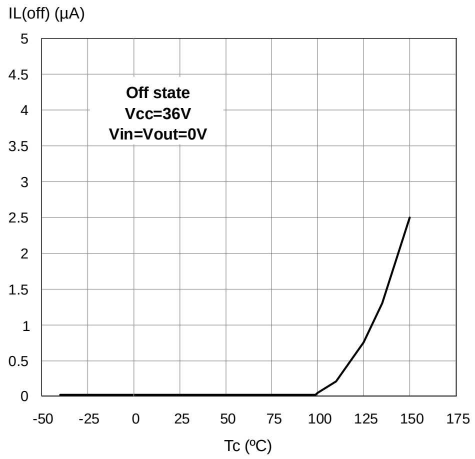
$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

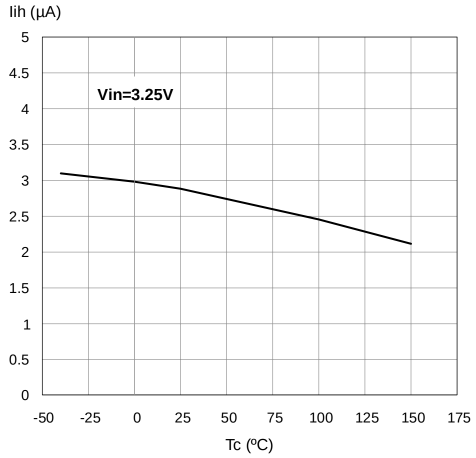
5kΩ ≤ R_{prot} ≤ 65kΩ.

Recommended R_{prot} value is 10kΩ.

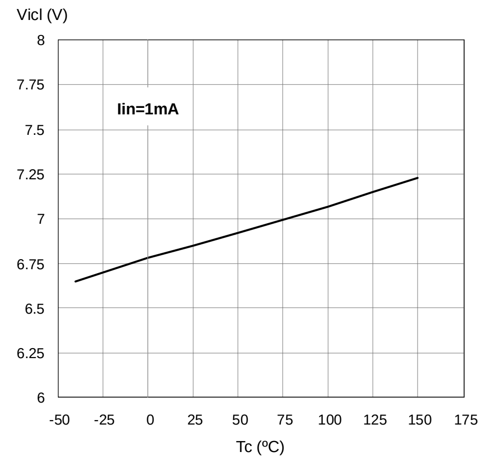
Off State Output Current



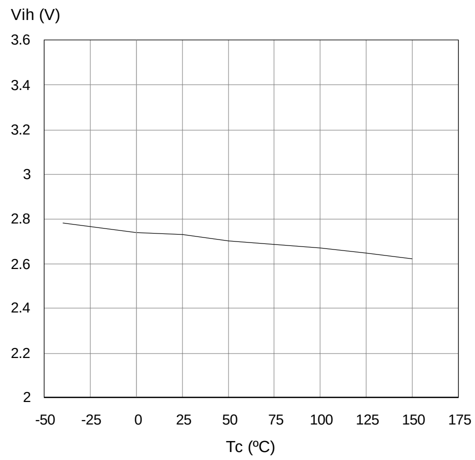
High Level Input Current



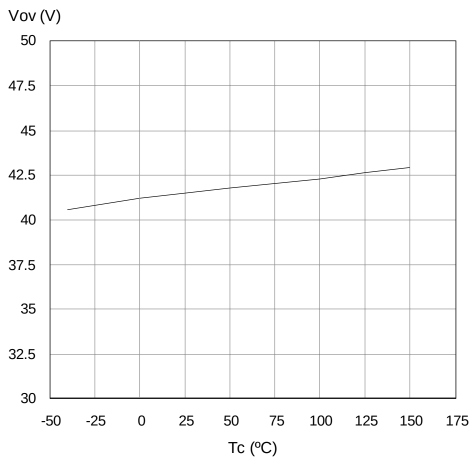
Input Clamp Voltage



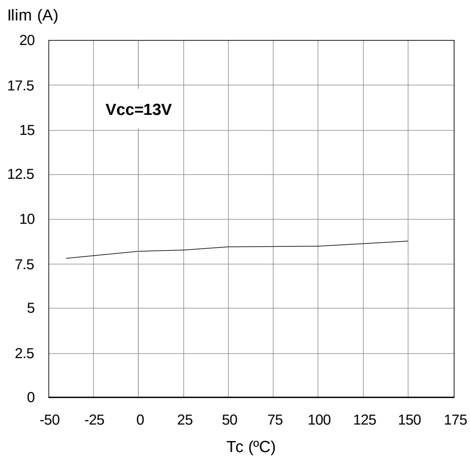
Input High Level



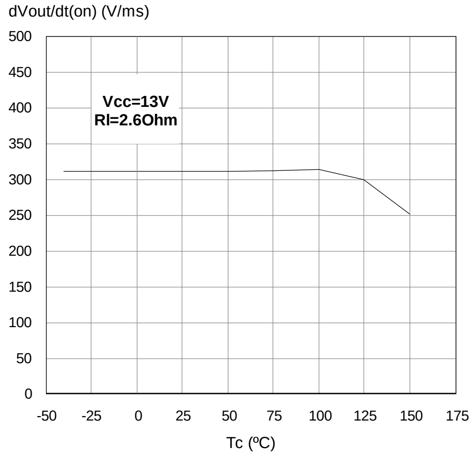
Overvoltage Shutdown



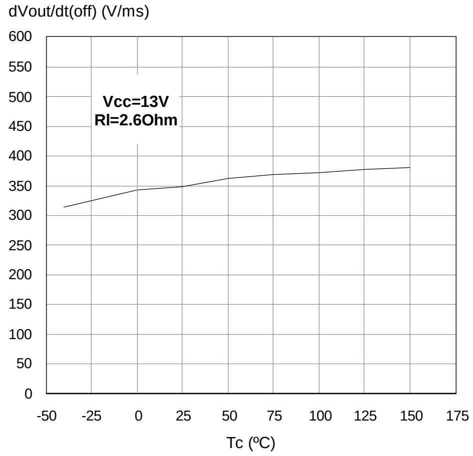
I_{LIM} Vs T_{case}



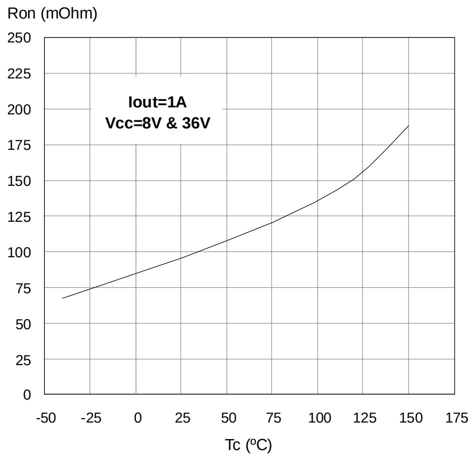
Turn-on Voltage Slope



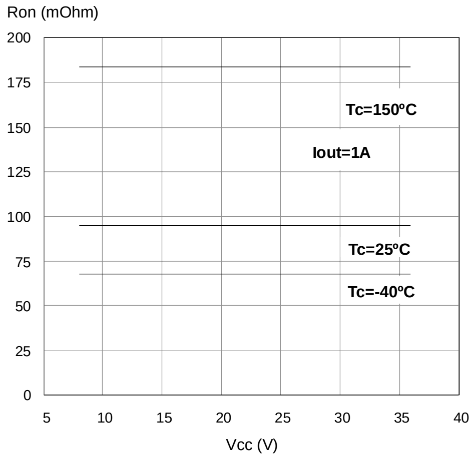
Turn-off Voltage Slope



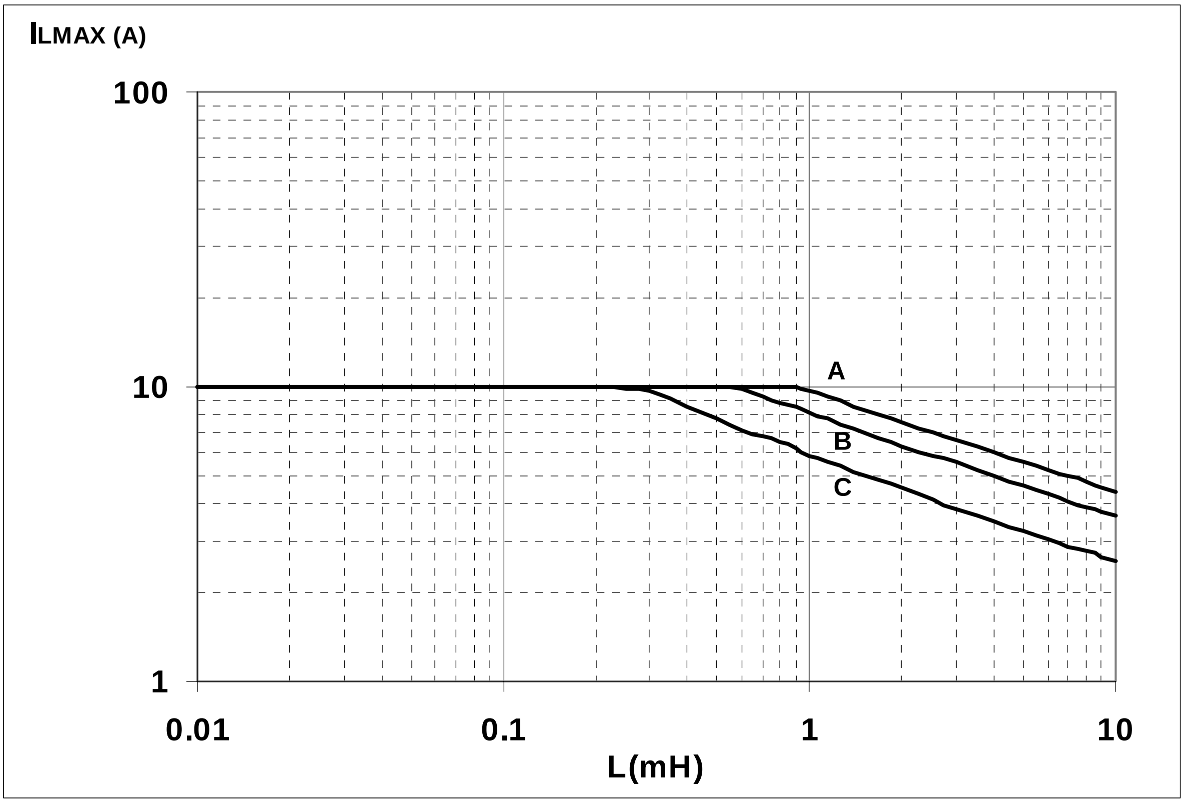
On State Resistance Vs T_{case}



On State Resistance Vs V_{CC}



Maximum turn off current versus load inductance



A = Single Pulse at T_{Jstart}=150ºC

B= Repetitive pulse at T_{Jstart}=100ºC

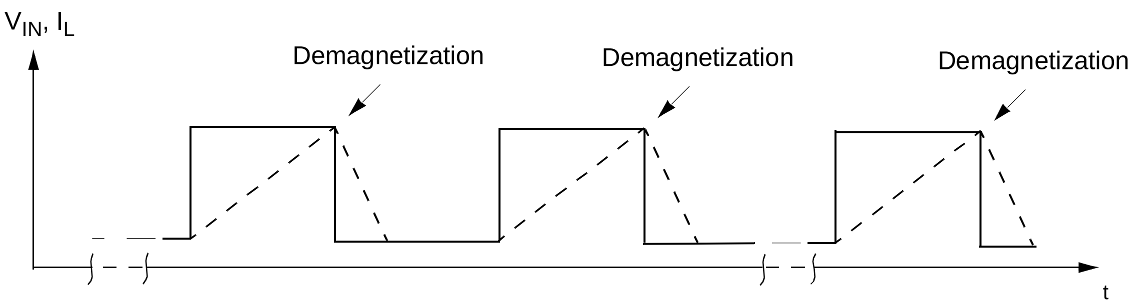
C= Repetitive Pulse at T_{Jstart}=125ºC

Conditions:

V_{CC}=13.5V

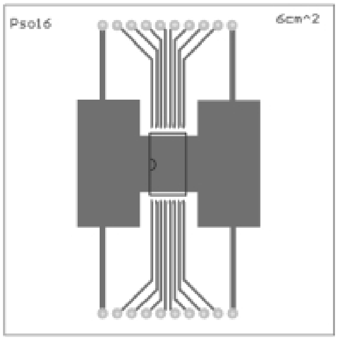
Values are generated with R_L=0Ω

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



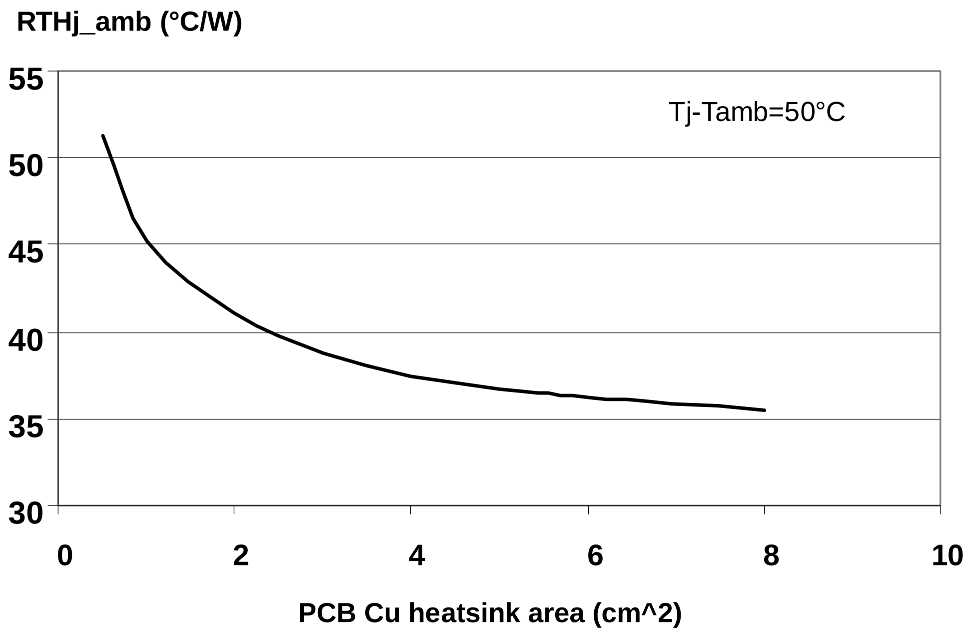
PowerSO-16™ THERMAL DATA

PowerSO-16™ PC Board

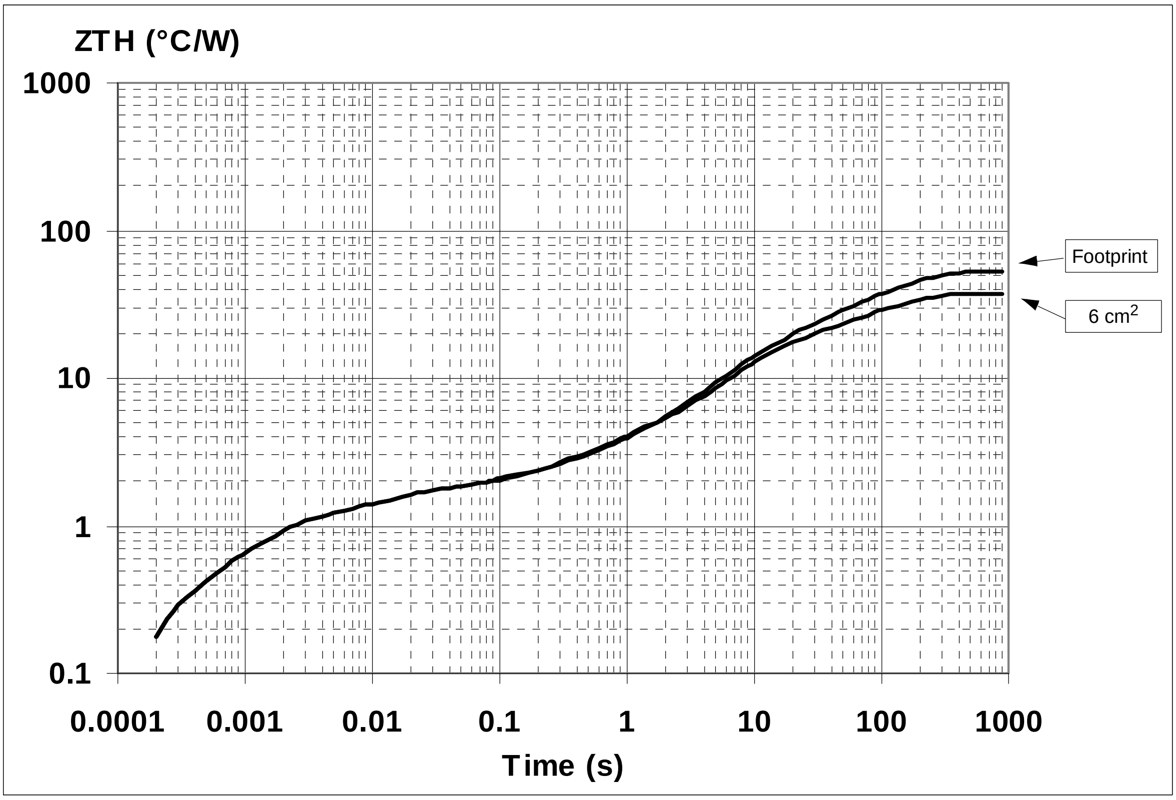


Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 60mm x 60mm, PCB thickness=2mm, Cu thickness=35µm, Copper areas: 6cm^2).

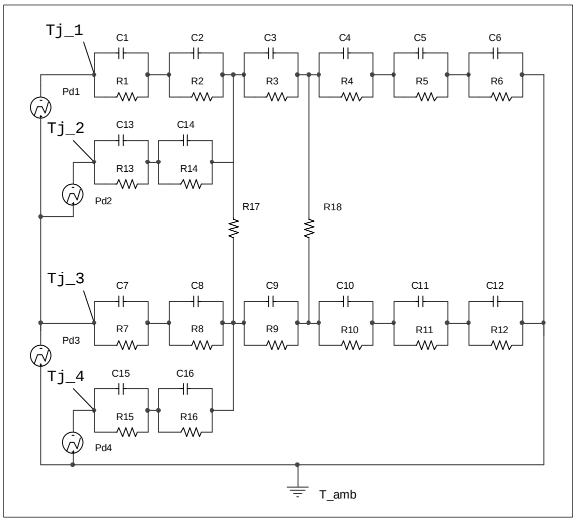
$R_{thj-amb}$ Vs PCB copper area in open box free air condition



Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a quad HSD in PowerSO-16



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

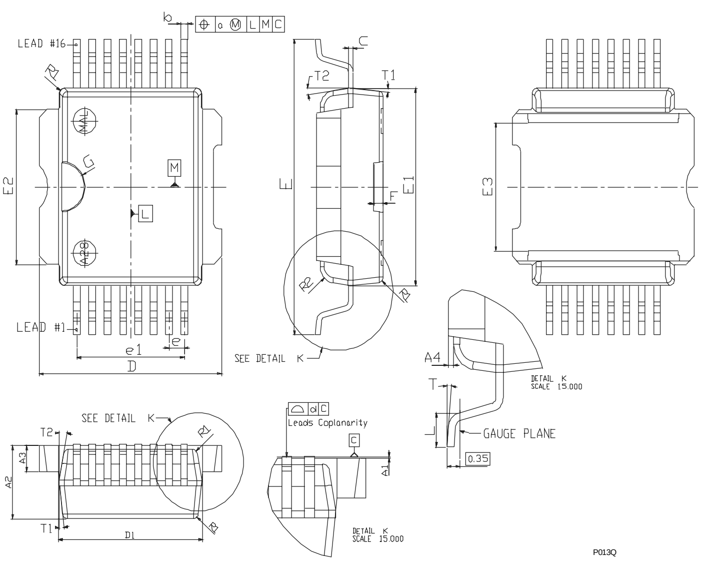
where $\delta = t_p / T$

Thermal Parameter

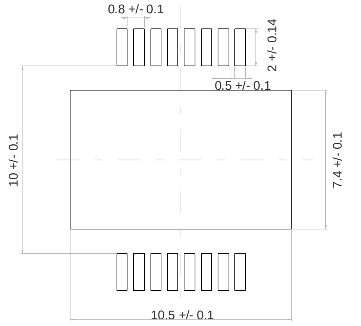
Area/island (cm^2)	Footprint	6
R1 (°C/W)	0.18	
R2 (°C/W)	0.8	
R3 (°C/W)	0.7	
R4 (°C/W)	0.8	
R5 (°C/W)	13	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0006	
C2 (W.s/°C)	1.50E-03	
C3 (W.s/°C)	1.75E-02	
C4 (W.s/°C)	0.4	
C5 (W.s/°C)	0.75	
C6 (W.s/°C)	3	5

POWERSO-16™ MECHANICAL DATA

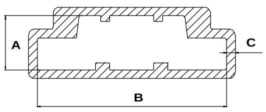
DIM.	mm.		
	MIN.	TYP	MAX.
A1	0	0.05	0.1
A2	3.4	3.5	3.6
A3	1.2	1.3	1.4
A4	0.15	0.2	0.25
a		0.2	
b	0.27	0.35	0.43
c	0.23	0.27	0.32
D	9.4	9.5	9.6
D1	7.4	7.5	7.6
d	0	0.05	0.1
E (1)	13.85	14.1	14.35
E1	9.3	9.4	9.5
E2	7.3	7.4	7.5
E3	5.9	6.1	6.3
e		0.8	
e1		5.6	
F		0.5	
G		1.2	
L	0.8	1	1.1
R1			0.25
R2		0.8	
T	2°	5°	8°
T1	6° (typ.)		
T2	10° (typ.)		
Package Weight	(typ.)		



PowerSO-16™ SUGGESTED PAD LAYOUT



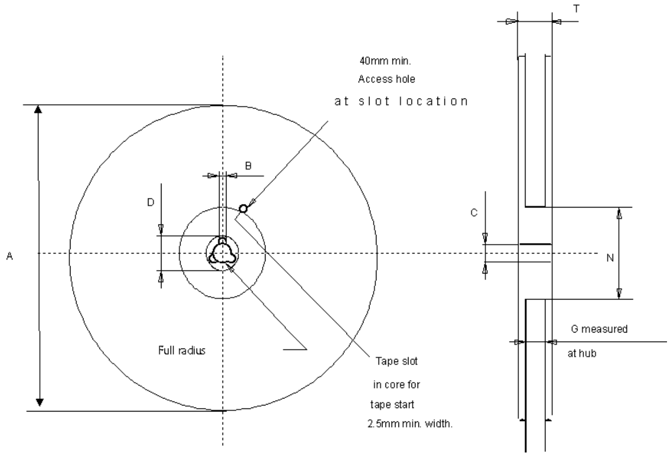
TUBE SHIPMENT (no suffix)



All dimensions are in mm.

Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
50	1000	532	4.9	17.2	0.8

TAPE AND REEL SHIPMENT (suffix "13TR")



REEL DIMENSIONS

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

All dimensions are in mm.

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	24
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.

